AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1.-11. (Cancelled)

12. (Currently Amended) A method of forming the integrated structure in claim [[1]]13 comprising the steps of:

providing said[[a]] substrate;

forming said first type device and said second type device positioned on said substrate, such that said uppermost surface of said first type device is higher than said uppermost surface of said second type device ~~a plurality of different height devices positioned on said substrate~~;

forming a passivating layer positioned above said substrate and between said first and second type devices;

removing an upper portion of said passivating layer to expose the uppermost surface of said first type device so that the top surface of said passivating layer has a height within approximately 50 nm of the uppermost surface of said first type device ~~top of at least one of the tallest of said plurality of devices~~ while leaving the second type device ~~shorter of said plurality of devices~~ covered by said passivating layer;

forming ~~said first~~ a second device contact embedded in said passivating layer, said second device contact having a top surface that is substantially coplanar with said top surface of said passivating layer, said ~~first~~ second device contact being electrically connected to said second type device ~~at least one of the shorter of said plurality of devices~~; and

forming a wiring layer above said passivating layer, ~~such that~~ said wiring layer comprising an insulating layer;

forming said first device contact embedded within said insulating layer of said wiring layer using a dedicated photolithographic mask; and

forming wires within said insulating layer of said wiring layer using a separate photolithographic mask from said dedicated photolithographic mask ~~is in direct contact with said top of said at least one of the tallest of said plurality of devices~~.

13. (New) An integrated circuit structure comprising:

a substrate;

a first type device and a second type device positioned on said substrate, said first type device having an uppermost surface that is higher than an uppermost surface of said second type device;

a passivating layer positioned above said substrate and between said first and second type devices, wherein said passivating layer has a top surface substantially coplanar with said uppermost surface of said first type device;

a wiring layer above said passivating layer comprising a first device contact embedded therein that is in electrical contact with said uppermost surface of said first type device;

a second device contact embedded within said passivating layer and in electrical contact with said second type device; and

a conductive wire feature embedded within said wiring layer, said conductive wire feature in electrical contact with said second device contact.

14. (New) The integrated circuit structure of claim 13, wherein said top surface of said passivating layer has a height within approximately 50 nm of the uppermost surface of said first type device.

15. (New) The integrated circuit structure of claim 13, wherein said first type device is a bipolar transistor.

16. (New) The integrated circuit structure of claim 15, wherein said first device contact is an emitter contact.

17. (New) The integrated circuit structure of claim 16, wherein said emitter contact comprises a different material than said conductive wire feature.

18. (New) The integrated circuit structure of claim 16, wherein said emitter contact comprises a material that is compatible with a chemical mechanical polishing process used on said conductive wire feature.

19. (New) The integrated circuit structure of claim 13, wherein said second type device is a CMOS transistor.